Remarks

In the instant Office Action dated January 2, 2008, claim 12 is objected to due to informalities, and the following rejections are listed: claims 1-4, 6, 10-23 and 27-29 stand rejected under 35 U.S.C. § 102(b) over Buer *et al.* (US Patent No. 6,114,880); claims 5, 8-9, and 25-26 stand rejected under 35 U.S.C. § 103(a) over Buer in view of Chuang *et al.* (US Patent Pub. 2003/0128606); and claims 7 and 24 stand rejected under 35 U.S.C. § 103(a) over Buer in view of Flautner *et al.* (US Patent No. 7,278,080).

In response to the objection to claim 12, Applicant has amended claim 12 in a manner consistent with that suggested by the Examiner. Thus, Applicant requests that the objection to claim 12 be removed.

Applicant respectfully traverses the § 102(b) rejection of claims 1-4, 6, 10-23 and 27-29 because the rejection relies upon the erroneous assertion that Buer's known path generation circuit 14 provides a predetermined reference signal to Buer's critical path logic 20. As is clearly shown by Buer in Figure 1 reproduced below, Buer's known path generation circuit 14 is in parallel to Buer's critical path logic 20 and, as such, no signals are provided from known path generation circuit 14 to critical path logic 20.

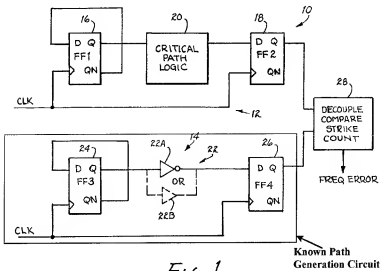

Fig. 1

According to M.P.E.P. § 2131, in order to anticipate a claim, the elements of a prior art reference must be arranged as required by the claim. In this instance, the claimed invention requires that the signal generator generate a reference signal which is provided by the signal generator to the duplicate logic path. As is clearly shown in Buer's Figure 1, none of the signals that are generated by known path generation circuit 14 (*i.e.*, the

Office Action's alleged signal generator) are provided to critical path logic 20 (*i.e.*, the Office Action's alleged duplicate logic path) because Buer's paths are arranged in parallel to each other. Thus, the cited portions of the Buer reference are not arranged as required by the claimed invention. Accordingly, the § 102(b) rejection of claims 1-4, 6, 10-23 and 27-29 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 11-12 and 29 because the cited portions of Buer do not correspond to aspects of the claimed invention directed to the duplicate logic path including one or more buffer stages. The Office Action cites to Buer's buffers 22 as allegedly corresponding to the claimed buffers of the duplicate logic path (*see, e.g.*, Figure 1 and Col. 3:64 to Col. 4:9); however, Buer teaches that buffers 22 are part of known path generation circuit 14, not part of critical path logic 20 (*i.e.*, the Office Action's alleged duplicate logic path). Accordingly, the § 102(b) rejection of claims 11-12 and 29 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 14 and 16 because the cited portions of Buer do not correspond to aspects of the claimed invention directed to the timing violation signal being supplied to a second timing closure monitoring circuit. The Office Action cites to Buer's protection circuit 30 as allegedly corresponding to the claimed second timing closure monitoring circuit; however, the cited portions of Buer do not teach that protection circuit 30 has a duplicate logic path of a logic path being monitored or that protection circuit 30 has a signal generator that generates a predetermined reference signal. Accordingly, the § 102(b) rejection of claims 14 and 16 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 5, 7-9 and 24-26 because the cited portions of the Buer reference do not correspond to the claimed invention as discussed above in relation to the § 102(b) rejection of claims 1 and 19. Applicant submits that neither the addition of the Chuang reference nor the addition of the Flautner reference overcome the above discussed deficiencies of Buer. In at least this regard, the § 103(a) rejections are improper. Accordingly, Applicant requests that the § 103(a) rejections of claims 5, 7-9 and 24-26 be withdrawn.

Applicant further submits that the § 102(b) and § 103(a) rejections cannot stand because the cited portions of Buer do not correspond to aspects of the claimed invention

directed to the monitoring circuit providing a timing closure signal indicative of the status of the timing closure in the logic path being monitored responsive to comparing receipt of the output signal of the duplicate logic path to receipt of the clock signal. The Office Action asserts that Buer's comparator circuit 28 corresponds to the claimed monitoring circuit; however, the cited portions of Buer teach that comparator circuit 28 compares the output of known path generation circuit 14 to the output of critical path generation circuit 12 to generate a frequency error signal. *See, e.g.,* Figure 1 and Col. 4:9-30. Thus, Buer's comparator circuit 28 does not compare the receipt of the output of the duplicate logic path to the receipt of the clock signal in order to produce the timing closure signal as in the claimed invention. Accordingly, Applicant requests that the § 102(b) and § 103(a) rejections be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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